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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,066	03/30/2006	Theodore J. Letavic	US03 0376 US2	9392

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
01/07/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/574,066	LETAVIC, THEODORE J.	
	Examiner	Art Unit	
	SAMUEL A. GEBREMARIAM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *6-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,22-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-5 and 22-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what the structural relationship is between the trench gate, source, body, and drain of the MOS device and the emitter, base and collector region and the bipolar device. Where the emitter, base and collector of the bipolar device in relation to MOS device? It appears from the description that it is the biasing of MOS device that causes the device to behave as a bipolar transistor structure, however there is no physical/permanent bipolar device that is shown in the figures. Therefore it is not clear how the trench gate, source, body and drain of the MOS device and the emitter, base and collector regions of the bipolar device are related.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warwick, US 2001/0023957.

Regarding claims 1 and 29-31, as best the examiner is able to ascertain the claimed invention, Warwick teaches a hybrid MOS-bipolar device comprising a trench MOS device having a source (13A), gate (21), where the gate (21) is a trench gate, drain (14) and body regions (15A). Since Warwick teaches a MOS device and since a MOS transistor has a parasitic bipolar transistor, Warwick teaches an emitter, a collector and base.

Warwick does not explicitly state that the gate and the body being shorted together and biased positively relative to the drain.

However shorting a gate and a body region is conventional and well known that is routinely practice to use transistors as breakdown diodes.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to short the body and the gate as claimed in the structure of Warwick, in order to use the MOS device as a breakdown diode.

Regarding claim 2, Warwick teaches substantially the entire claimed structure of claim 1 above except explicitly stating that a gate oxide having has a single oxide thickness of under 600A.

Parameters such as oxide thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the oxide thickness as claimed in the structure of Warwick, in order to use the MOS device as a breakdown diode.

Regarding claim 3, Warwick teaches substantially the entire claimed structure of claim 1 above including a gate oxide having multiple oxide thicknesses for formation of gate and field-oxide regions (Warwick teaches device isolation regions).

Regarding claim 4, Warwick teaches substantially the entire claimed structure of claim 1 above including a square trench geometry (figs. 6 and 7).

Regarding claim 5, Warwick teaches substantially the entire claimed structure of claim 1 above including the trench gate having a circular geometry (circular trench gates are well known).

Regarding claims 22-27, as best the examiner is able to ascertain the claimed invention, Warwick teaches a hybrid MOS-bipolar device comprising: a MOS device having a trench gate (21), a source (13a), a drain (14) and a body (15); a bipolar device having an emitter, a collector, a base and a gate formed by the trench gate, the emitter and the source being formed by a common region (Warwick teaches a MOS device and since a MOS transistor has a parasitic bipolar transistor, Warwick teaches an emitter, a collector and base), the base and the body being formed by a common region, and the collector and the drain being formed by a common region; a substrate that includes a PI region and an N drift region, the trench gate extending from a top surface of the substrate through the PI region into the N drift region; a first electrode coupled to the

trench gate, the body and the base; and a second electrode coupled to the source and the emitter.

Warwick does not explicitly state that the gate and the body being shorted together and biased positively relative to the drain.

However shorting a gate and a body region is conventional and well known that is routinely practice to use transistors as breakdown diodes.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to short the body and the gate as claimed in the structure of Warwick, in order to use the MOS device as a breakdown diode.

Response to Arguments

5. Applicant's arguments filed 9/11/09 have been fully considered but they are not persuasive. Applicant's argument the 112 2nd paragraph rejections rely upon the same erroneous rationale as the 112 1st rejections rely upon and similarly improper reasons as discussed above. In response, the 112 1st paragraph rejection was based upon the specification not providing support to the limitations of a MOS device having source, body, and drain of the MOS device and the emitter, base and collector region and the bipolar device. As highlighted by applicant [0010-0011] provides support for this type of device. However the 112 2nd paragraph is still maintained, because it appears from the description that it is the biasing of MOS device that causes the device to behave as a bipolar transistor structure. There is no physical/permanent bipolar device that is shown in the figures. Therefore it is not clear how the trench gate, source, body and drain of the MOS device and the emitter, base and collector regions of the bipolar device are

related. Furthermore since Warwick teaches similar device as claimed, Warwick's

structure could be properly biased to provide a bipolar device as claimed.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/SAG/

December 29, 2009